INDUCTIVE VOLTAGE ADDER NETWORK ANALYSIS AND MODEL SIMPLIFICATION*

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Abstract

Inductive voltage adder topology has attracted great attentions in pulse power community for near two decades. However, there has been lack of literatures on inductive voltage adder network analysis and circuit design model. We have recently developed a simplified model and a set of simple formulas. An expanded model and more detailed analysis are presented in this paper. Our model reveals the relationship of output waveform parameters and hardware designs. Computer simulations have demonstrated that parameter estimation based on this approach is accurate. This approach can be used in early stages of project development to assist feasibility study, geometry selection in engineering design, and parameter selection of critical components. A set of fundamental estimation formulas including system impedance, rise time, and number of stages are presented. This approach is also applicable to induction LINAC design. In addition, the model presented in this paper shows a new topology of high voltage waveform generator.

I. INTRODUCTION

In our earlier papers [1] and [2] , we presented an inductive voltage adder (IVA) transmission network model based on circuit element simplification approach and a set of estimation formulas derived from the model. It was the first step to reveal IVA mechanism. They are intended for industrial applications.

We introduce here an expanded model and a more formal approach of IVA analysis.

II. SIMPLIFICATION

A single cell circuit model of inductive voltage adder, shown in Figure 1., was given in [3] and [4]. Where, SW is the main switch, C_S is the capacitance of energy storage capacitor, R is the parallel resistor, L_K is core leakage inductance, L_P is primary core inductance, and L_1 and C_1 are the distributed inductance and capacitance of stalk per stack section length.

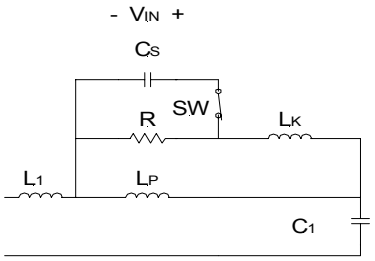

Figure 1. A single cell model of inductive voltage adder

When storage capacitors are large enough to keep constant voltage, they can be substituted by batteries in the circuit model. The switch and large capacitor, or a battery, can be represented by a "step input" source of voltage V_{IN}, where V_{IN} is the initial voltage of storage capacitors. Therefore, a single-stack inductive voltage adder model can be replaced by a new one as shown in Figure 2.

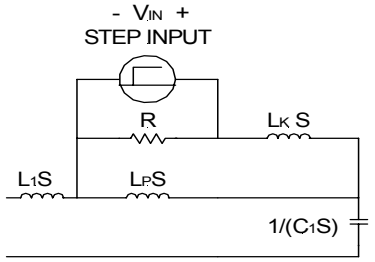

Figure 2. A single stack model of inductive voltage adder with step input

In each stack cell, the resistor R is in parallel with the input source of zero impedance hence it can be eliminated, as shown in Figure 3.

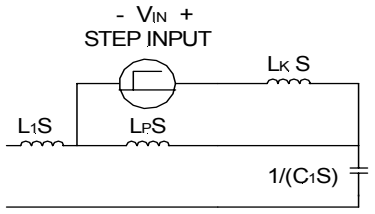

Figure 3. A single stack model of inductive voltage adder with step input and R eliminated

* Work performed under auspices of the US Dept. of Energy.
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Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
JUN 2007	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Inductive Voltage Adder Network Analysis And Model Simplification	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Brookhaven National Laboratory Upton, NY 11973 USA**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002371. 2013 IEEE Pulsed Power Conference, Digest of Technical Papers 1976-2013, and Abstracts of the 2013 IEEE International Conference on Plasma Science. IEEE International Pulsed Power Conference (19th). Held in San Francisco, CA on 16-21 June 2013., The original document contains color images.

14. ABSTRACT
Inductive voltage adder topology has attracted great attentions in pulse power community for near two decades. However, there has been lack of literatures on inductive voltage adder network analysis and circuit design model. We have recently developed a simplified model and a set of simple formulas. An expanded model and more detailed analysis are presented in this paper. Our model reveals the relationship of output waveform parameters and hardware designs. Computer simulations have demonstrated that parameter estimation based on this approach is accurate. This approach can be used in early stages of project development to assist feasibility study, geometry selection in engineering design, and parameter selection of critical components. A set of fundamental estimation formulas including system impedance, rise time, and number of stages are presented. This approach is also applicable to induction LINAC design. In addition, the model presented in this paper shows a new topology of high voltage waveform generator.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**SAR**	**4**	

Comparing impedance of two parallel branches of L_K and L_P, the leakage inductance L_K is usually much, much smaller than the primary inductance L_P, so is its impedance. Therefore, the circuit branch of L_P can be eliminated in analysis. The single cell inductive voltage adder model is simplified as shown in Figure 4.

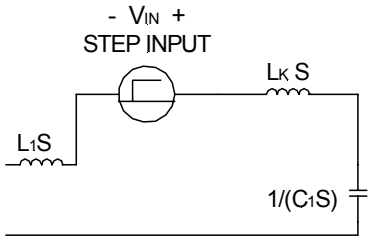

Figure 4. A simplified single stack model of inductive voltage adder with step input

The single cell model given in Figure 1 is unsymmetrical. We change this model to a symmetrical one as in Figure 5.

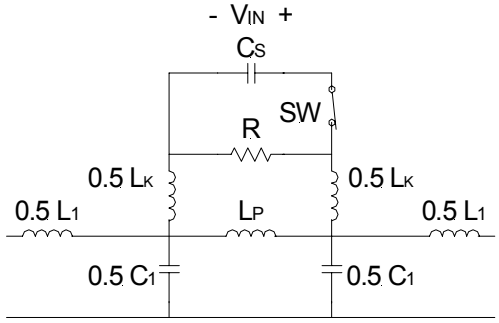

Figure 5. A symmetrical style single stack model

Its corresponding simplified model is given in Figure 6.

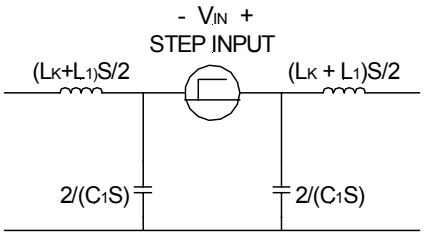

Figure 6. A symmetrical style simplified single stack model of inductive voltage adder with step input

III. NETWORK ANALYSIS AND DESIGN FORMULAS

The multi-stack inductive voltage adder is shown in Figure 7. The model is a ladder network of multiple "step input" sources.

Since the ideal step voltage source shall have zero impedance, the network transmission impedance of inductive voltage adder based on the circuit model of Figure 7 is then given by

$$Z = \sqrt{\frac{L_K + L_1}{C_1}} \tag{1}$$

This result shows that the circuit output impedance is larger than the stalk impedance due to the contribution of the leakage inductance. In order to minimize pulse reflections, the output cable and load shall match to the circuit output impedance Z rather then the stalk impedance.

The transmission delay time per stack cell is simply the propagation time of each transmission line section. It is given by

$$T_C = \sqrt{(L_1 + L_K)C_1} \tag{2}$$

Each stack cell has a natural resonant frequency of

$$\omega_O = \frac{1}{\sqrt{(L_1 + L_K)C_1}} \tag{3}$$

Commonly used configuration of inductive voltage adder is shown in Figure 8

Figure 8. Common configuration of multi-stack inductive voltage adder

It is called a single-ended IVA, if one of the load, ZL or ZR, is a short and the other one is matched to IVA transmission impedance Z. It is called a double-ended IVA, if both loads are identical and equal and matched to IVA transmission impedance Z.

Assuming all step input here has a voltage V_{IN} as in previous section, and ZL is a short and ZR equals to Z. The load voltage of single-ended matched IVA can be expressed as

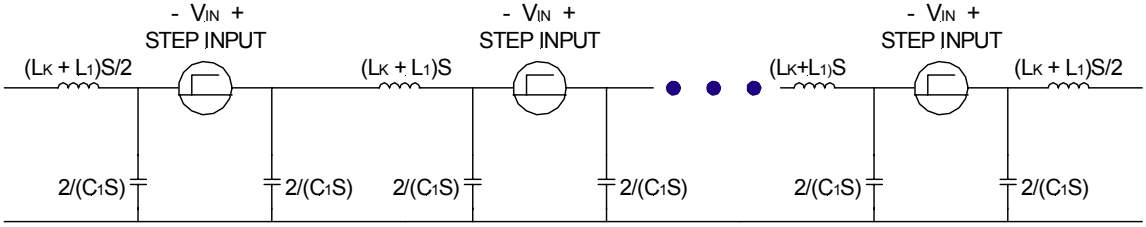

Figure 7. A symmetrical style simplified multi-stack model of inductive voltage adder with step input

$$V_{load} = NV_{IN} \quad (4)$$

Where V_{load} denotes output voltage across load ZR and N is number of stacks. The response voltage or current rise time, T_R, of single-ended matched IVA can be expressed as

$$T_R = 2N\sqrt{(L_K + L_1)C_1} \quad (5)$$

Similarly, the load voltage of either end, V_{Dload}, of double-ended matched IVA can be expressed as

$$V_{Dload} = \pm\frac{NV_{IN}}{2} \quad (6)$$

Where, V_{Dload} is positive for ZR and negative for ZL. The load voltage or current rise time, T_{DR}, of a double-ended matched IVA can be expressed as

$$T_{RD} = N\sqrt{(L_K + L_1)C_1} \quad (7)$$

Here C_1 and L_1 are stalk capacitance and inductance, and L_K is leakage inductance. They serve as transmission line elements during pulse propagation.

It is interesting to note distinctive differences of inductive-voltage-adder (IVA) and pulse-forming-network (PFN).

1. The output voltage of IVA is linearly dependent of number of stack cells, but output voltage of PFN is independent of number of cells.
2. The pulse rise time of IVA is linearly dependent of number of stack cells, but pulse rise time of PFN is independent of number of cells.
3. The pulse length of IVA is independent of number of stack cells, but PFN pulse length is dependent of number of cells.

IV. APPLICATION EXAMPLES

To demonstrate design application, we show a few simulation examples. Simulation parameters are from an actual circuit given in [3]. All switches are assumed to be ideal and identical.

TABLE 1 SIMULATION PARAMETERS

Symbol	Parameter	Quantity
C_S	storage capacitance	24×10^{-6} F
L_P	primary inductance	20.9×10^{-6} H
L_K	leakage inductance	6.5×10^{-9} H
L_1	stalk inductance per stake	20×10^{-9} H
C_1	stalk capacitance	2.6×10^{-12} F
N	number of stakes	30, 20, 10
V_0	initial voltage of C_S	1000 V
R	parallel resistance	50
Z_{STALK}	stalk impedance	50

From the above parameters, we can calculate the load impedance as

$$Z = \sqrt{\frac{L_K + L_1}{C_1}} = \sqrt{\frac{(6.5+20)\times10^{-9}}{2.6\times10^{-12}}} = 100.96\,\Omega \quad (8)$$

Here, the calculated load impedance is about twice of the stalk impedance.

Assuming a single-ended 30 stack IVA where ZL is a short, the voltage pulse rise time across ZR can be estimated by using equation (5).

$$T_R = 2\times30\sqrt{(20+6.5)\times2.6\times10^{-21}} = 15.75\ ns \quad (9)$$

Using equation (6), we have the estimated output load voltage of the single-ended IVA

$$V_{load} = 30\times1000\ V = 30\ kV \quad (10)$$

The simulation result is in Figure 10. A comparison of matched and mismatched impedance cases are shown in Figure 11, which illustrate effects on pulse waveforms.

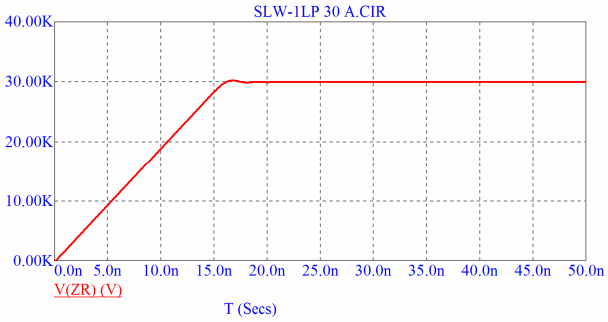

Figure 9. The output pulse waveform of a 30-stack single-ended IVA

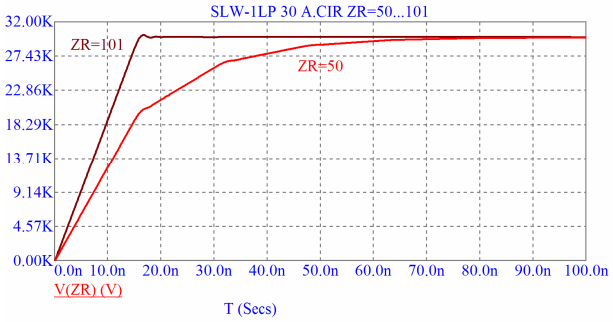

Figure 10. Output pulse waveforms of a 30-stack single-ended IVA with matched or mismatched impedance

Here we shown a set of simulation examples of double-ended IVA of 10, 20, or 30 stacks with switch on at 0.1 ns and off at 40 ns. The estimated parameters shown in Table 2 are calculated using equations given in the previous section. Simulation results and estimated parameters are well agreed.

TABLE 2 ESTIMATED DESIGN PARAMETERS

Symbol	Parameter	Quantity			
N	Number of stacks	10	20	30	
T_{RD}	Pulse rise time	2.62	5.25	7.87	ns
V_{Dload}	Pulse voltage	5	10	15	kV

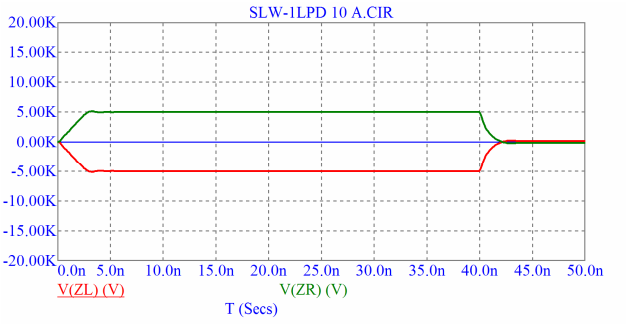

Figure 11. Output pulse waveforms of a 10-stack double-ended IVA

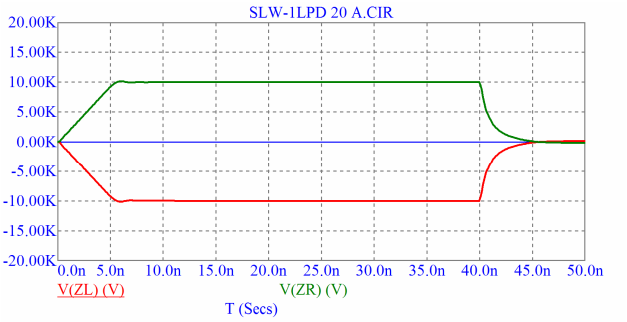

Figure 12. Output pulse waveforms of a 20-stack double-ended IVA

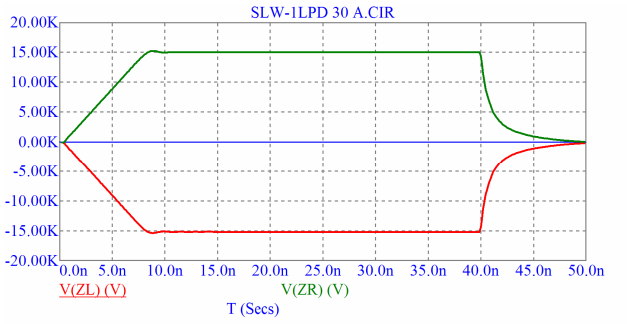

Figure 13. Output pulse waveforms of a 30-stack double-ended IVA

The circuit model is given in Figure 14.

V. CONCLUSION

The method introduced in this paper can be further extended to high voltage function generator design. We have build and tested a model function generator based on inductive voltage adder.

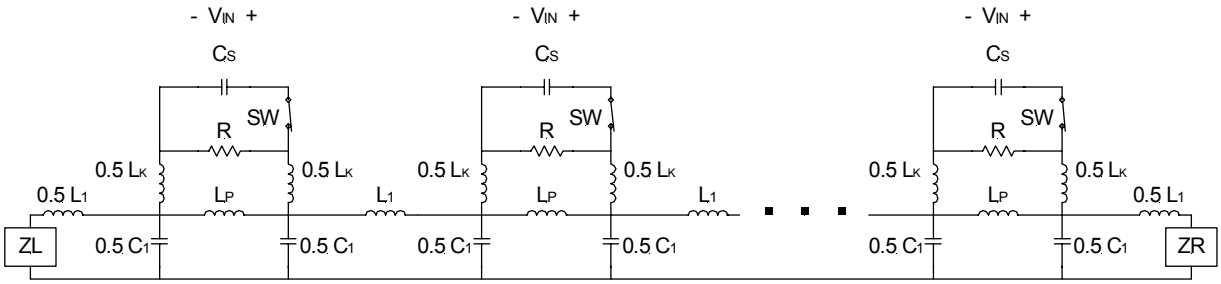

Figure 14. Example of IVA simulation model

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